THAT WHICH IS CLAIMED IS:

1. A method for controlling flow of network data arranged in frames and minimizing congestion, comprising the steps of:

generating a status error indicator within a FIFO memory of a network device indicative of a frame overflow within the FIFO memory;

in response to the status error indicator, generating an early congestion interrupt to a host processor indicative that a frame overflow has occurred within the FIFO memory;

discarding the incoming frame that has caused the frame overflow within the FIFO memory; and

enhancing the servicing of frames received within the FIFO memory by one of either increasing the number of words of a direct memory access (DMA) unit burst size or modifying the time-slice of other active processes.

2. A method according to Claim 1, and further comprising the step of generating an early congestion interrupt from the FIFO memory to a communications processor after generating the status error indicator.

3. A method according to Claim 2, and further comprising the step of setting early congestion notification bits within an interrupt register of a direct memory access unit from control signals generated by the communications processor.

4. A method according to Claim 3, and further comprising the step of generating from the direct memory access unit an early congestion

notification interrupt to a host processor to discard the incoming frame that has caused the frame overflow within the FIFO memory.

5. A method according to Claim 3, and further comprising the step of generating the early congestion notification interrupt from the direct memory access unit along a system bus.

6. A method according to Claim 1, and wherein the status error indicator is generated by generating a status error bit.

7. A method according to Claim 6, wherein the status error bit is generated by setting a flip-flop.

8. A method according to Claim 1, wherein the step of generating the status error indicator within the FIFO memory further comprises the step of setting an overflow bit within the FIFO memory indicative of an overflow condition.

9. A method for controlling flow of network data arranged in frames and minimizing congestion, comprising the steps of:

generating a status error indicator within a FIFO memory of a network device indicative of a frame overflow within the FIFO memory;

in response to the status error indicator, generating an early congestion interrupt to a host processor indicative that a frame overflow has occurred within the FIFO memory; and

discarding the incoming frame that has caused the frame overflow within the FIFO memory.

10. A method according to Claim 9, and further comprising the step of setting early congestion notification bits within an interrupt register of a direct memory access unit in the network device after generating the status error indicator within the FIFO memory.

11. A method according to Claim 10, and further comprising the step of generating from the direct memory access unit an early congestion notification interrupt to the host processor to discard the incoming frame that has caused the frame overflow within the FIFO memory.

12. A method according to Claim 10, and further comprising the step of generating the early congestion notification interrupt from the direct memory access unit along a system bus.

13. A method according to Claim 9, and wherein the status error indicator is generated by generating a status error bit.

14. A method according to Claim 9, wherein the status error bit is generated by setting a flip-flop.

15. A method according to Claim 9, wherein the step of generating the status error indicator within the FIFO memory further comprises the step of setting an overflow bit within the FIFO memory indicative of an overflow condition.

16. A method for controlling flow of network data arranged in frames and minimizing congestion, comprising the steps of:

generating a status error indicator within a FIFO memory of a network device indicative of a frame overflow within the FIFO memory;

generating from the FIFO memory an early congestion interrupt to a communications processor in response to the status error indicator;

processing the interrupt and setting at least one early congestion notification bit within an interrupt register of a direct memory access unit;

generating an early congestion interrupt from the direct memory access unit to a host processor indicative that a frame overflow has occurred within the FIFO memory; and

generating instructions from the host processor to the FIFO memory to discard the incoming frame that has caused the frame overflow.

17. A method according to Claim 16, and further comprising the step of generating the early congestion notification interrupt from the direct memory access unit along a system bus.

18. A method according to Claim 16, and wherein the status error indicator is generated by generating a status error bit.

19. A method according to Claim 18, wherein the status error bit is generated by setting a flip-flop.

20. A method according to Claim 16, wherein the step of generating the status error indicator

within the FIFO memory further comprises the step of setting an overflow bit within the FIFO memory indicative of an overflow condition.

21. A method for controlling flow of network data arranged in frames and minimizing congestion, comprising the steps of:

generating a status error indicator within a FIFO memory of a network device indicative of a frame overflow within the FIFO memory;

generating from the FIFO memory an early congestion interrupt to a communications processor of the network device in response to the status error indicator;

processing the interrupt and setting at least one early congestion notification bit within an interrupt register of a direct memory access unit of the network device;

generating an early congestion interrupt from the direct memory access unit to a host processor indicative that a frame overflow has occurred within the FIFO memory;

generating instructions from the host processor to the FIFO memory to discard the incoming frame that caused the frame overflow; and

enhancing the servicing of received frames by one of either increasing the number of words of a direct memory access (DMA) unit burst size or modifying the time-slice of other active processes.

22. A method according to Claim 21, and further comprising the step of generating the early congestion notification interrupt from the direct memory access unit along a system bus.

23. A method according to Claim 21, and wherein the status error indicator is generated by generating a status error bit.

24. A method according to Claim 23, wherein the status error bit is generated by setting a flip-flop.

25. A method according to Claim 21, wherein the step of generating the status error indicator within the FIFO memory further comprises the step of setting an overflow bit within the FIFO memory indicative of an overflow condition.

26. An apparatus for controlling flow of network data arranged in frames and minimizing congestion comprising:

a FIFO memory, including means for generating a status error indicator indicative of a frame overflow within the FIFO memory;

a direct memory access unit having an interrupt register and early notification bits that are set in response to the status error indicator corresponding to the overflow within the FIFO memory;

means for generating an early congestion interrupt from the direct memory access unit;

a host processor for receiving the early congestion interrupt from the direct memory access unit; and

means for generating instructions from the host processor to the FIFO memory to discard the incoming frame that has caused the frame overflow.

27. An apparatus according to Claim 26, and further comprising a system bus connecting the direct

memory access unit with the host processor and on which the early congestion notification interrupt passes.

28. An apparatus according to Claim 26, wherein the status error indicator comprises a status error bit.

29. An apparatus according to Claim 26, and further comprising a flip-flop that is set to indicate the status error bit.

30. An apparatus according to Claim 26, and further comprising means for setting an overflow bit within the FIFO memory indicative of the overflow condition.

31. An apparatus for controlling flow of network data arranged in frames and minimizing congestion comprising:

a FIFO memory, including means for generating a status error indicator indicative of the frame overflow within the FIFO memory;

a direct memory access unit having an interrupt register and early notification bits that are set in response to the status error indicator corresponding to the overflow within the FIFO memory;

means for generating an early congestion interrupt from the direct memory access unit;

a host processor for receiving the early congestion interrupt from the direct memory access unit;

means for generating instructions from the host processor to the FIFO memory to discard the incoming frame that has caused the frame overflow; and

means for enhancing the servicing of received frames by one of either increasing the number of words of a direct memory access (DMA) burst size or modifying the time-slice of other active processes.

32. An apparatus according to Claim 31, and further comprising a system bus connecting the direct memory access unit with the host processor and on which the early congestion notification interrupt passes.

33. An apparatus according to Claim 31, wherein the status error indicator comprises a status error bit.

34. An apparatus according to Claim 31, and further comprising a flip-flop that is set to indicate the status error bit.

35. An apparatus according to Claim 31, and further comprising means for setting an overflow bit within the FIFO memory indicative of the overflow condition.

36. A network device for controlling network data congestion, comprising:

means for generating a status error indicator within a FIFO memory indicative of a frame overflow within the FIFO memory;

means for reading the status error indicator and, in response, generating an early congestion interrupt to a host processor indicative that a frame overflow has occurred within the FIFO memory; and

means for discarding the incoming frame that has caused the frame overflow within the FIFO memory.

37. A network device according to Claim 36, and further comprising a direct memory access unit, and further comprising an interrupt register having early congestion notification bits that are set to indicate the overflow condition.